CLAIMS

1. A device for the emulation of designs for integrated circuits having a receiving device (1, 2, 3, 4, 5, 6) for multiple programmable logic circuits (11, 12, 13; 21, 22, 23), particularly FPGAs, and an electrical connection structure (14; 24), which has bus lines (111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232), each of which includes multiple channels (1...k),

characterized in that,

- each programmable logic circuit (11, 12, 13; 21, 22, 23) is connected to at least one bus line (111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232) and
- the connection structure (14; 24) is implemented so it may be flexibly interconnected,
  - in that the assignment of at least a part of the terminal contacts of any programmable logic circuit (11, 12, 13; 21, 22, 23) is freely programmable and
  - in that at least a part of the bus lines (111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232) connected to the programmable logic circuits (11, 12, 13; 21, 22, 23) are alternately electrically connectable to one another in such a way that at least one channel (1...k) of a bus line (111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232) is electrically connectable to a channel (1...k) of at least one other bus line (111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232) using a switch (S_1...S_k).

2. The device according to Claim 1,

characterized in that multiple channels (1...k) of a bus line (111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232) are alternately electrically connectable to multiple channels (1...k) of another bus line (111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232), each channel (1...k) of the one bus line (111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232) being electrically connectable to the assigned channel (1...k) of the other bus line (111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232), the individual channels (1...k) being connectable independently of one another.

3. The device according to Claim 1 or 2,

characterized in that connection bus lines (15, 16, 17; 25, 26, 27) are provided between at least a part of the programmable logic circuits (11, 12, 13; 21, 22, 23) for direct connection of the corresponding logic circuits (11, 12, 13; 21, 22, 23).

4. The device according to one of the preceding claims,

characterized in that multiple receiving devices (1, 2; 3,4; 5,6) are connectable to one another via connection devices (7A, 7B, 7C; 9A, 9B), the connection devices (7A, 7B, 7C; 9A, 9B) having switchable bus lines.

5. The device according to Claim 4,

characterized in that main connection devices (7A, 7B, 7C) are provided, each of which connects two receiving devices (1, 2; 3,4; 5,6) to one another, the main connection devices (7A, 7B, 7C) having bus lines (711,

712, 721, 722, 731, 732), which connect the particular bus lines (111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232) of the two receiving devices (1, 2) assigned to one another to one another and the bus lines (711, 712, 721, 722, 731, 732) of a main connection device (7A, 7B, 7C) being alternately electrically connectable to one another in such a way that at least one channel (1...k) of a bus line (711, 712, 721, 722, 731, 732) is electrically connectable to the channel (1...k) of at least one other bus line (711, 712, 721, 722, 731, 732).

6. The device according to Claim 5,

characterized in that group connection devices (9A, 9B) are provided, each of which connects two receiving device pairs, including two receiving devices (1, 2; 3,4; 5,6), connected to one another using a main connection device (7A, 7B, 7C), to one another and a group connection device (9A; 9B) having bus lines (911, 912, 913, 914, 915, 916), which are connected to the bus lines of the particular receiving device pair (1, 2; 3, 4; 5, 6), and the bus lines (911, 912, 913, 914, 915, 916) of the group connection devices (9A, 9B) each being switchable in such a way that each channel (1...k) of each bus line (911, 912, 913, 914, 915, 916) of the group connection device (9A, 9B) is assigned a switch (S_1...S_k) and the particular switches may be switched on and off independently of one another.

7. The device according to one of the preceding claims,

characterized in that the receiving devices (1, 2, 3, 4, 5, 6), the main connection devices (7A, 7B, 7C), and the group connection devices (9A, 9B) have circuit boards (10, 20, 30, 40, 50, 60; 70A, 70B, 70C; 90A,

90B), which are provided on their upper side and on their lower side with plug connector arrangements (V_O, V_U) which include multiple plug connectors situated in the same position on the particular circuit board (10, 20, 30, 40, 50, 60; 70A, 70B, 70C; 90A, 90B) and the outward-leading bus lines of the particular circuit board (10, 20, 30, 40, 50, 60; 70A, 70B, 70C; 90A, 90B) are electrically connected to both upper and corresponding lower plug connectors of the particular plug connector arrangement (V_O, V_U) in the same way.

8. The device according to Claim 7,

characterized in that the circuit boards (10, 20, 30, 40, 50, 60; 70A, 70B, 70C; 90A, 90B) are positioned one over another and are mechanically and electrically connected to one another using the plug connector arrangements (V_O, V_U), two circuit boards (10, 20, 30, 40, 50, 60) at a time of the receiving devices (1, 2; 3,4; 5,6) being connected like a sandwich into a receiving device pair using a circuit board (70A, 70B, 70C) of a main connection device (7A, 7B, 7C) positioned between them and the receiving device pairs being connected to one another using the circuit boards (90A, 90B) of the group connection devices (9A, 9B).

9. The device according to Claim 7 or 8,

characterized in that spacing (L) is provided between some of the plug connectors of the particular plug connector arrangements (V_O, V_U), which allows cool air to flow through the circuit board sandwich between the plug connectors.

10. A computer program for flexible interconnection of the connection structure of a device for the emulation of

designs for integrated circuits according to one of the preceding claims,

characterized in that the computer program executes the following program steps:

- checking whether elements having a placement setting are provided in the design of an integrated circuit to be emulated;
- if elements of this type are provided, assigning a slot of the receiving device for the particular element;
- assigning a particular slot for a particular element without a placement setting;
- checking whether signals are to be exchanged between the elements and/or with external expansion elements via predetermined terminal contacts;
- if so, assigning the particular terminal contacts to one another via corresponding channels of the bus lines;
- routing the remaining signals to be exchanged;
- calculating the internal and external assignment of the terminal contacts of the logic circuits;
- producing the internal connections between the integrated circuit design to be emulated and the assigned terminal contacts of each programmable logic circuit, and
- producing the external connections between the terminal contacts of the programmable logic circuits and the assigned channels of the bus lines.